LMP8601 LMP8601-Q1 60-V Common-Mode Bidirectional Precision Current Sensing Amplifier

Check for Samples: LMP8601, LMP8601-Q1

FEATURES

- **Unless Otherwise Noted, Typical Values at T_A = 25°C, V_S = 5.0V, Gain = 20x**
  - **TCV_{OS} 10µV/°C Max**
  - **CMRR 90 dB Min**
  - **Input offset voltage 1 mV Max**
  - **CMVR at V_S = 3.3V -4V to 27V**
  - **CMVR at V_S = 5.0V -22V to 60V**
  - **Operating Ambient Temperature Range -40°C to 125°C**
  - **LMP8601Q Available in Automotive AEC-Q100 Grade 1 Qualified Version**
  - **Single-Supply Bidirectional Operation**
  - **All Min / Max Limits 100% Tested**

APPLICATIONS

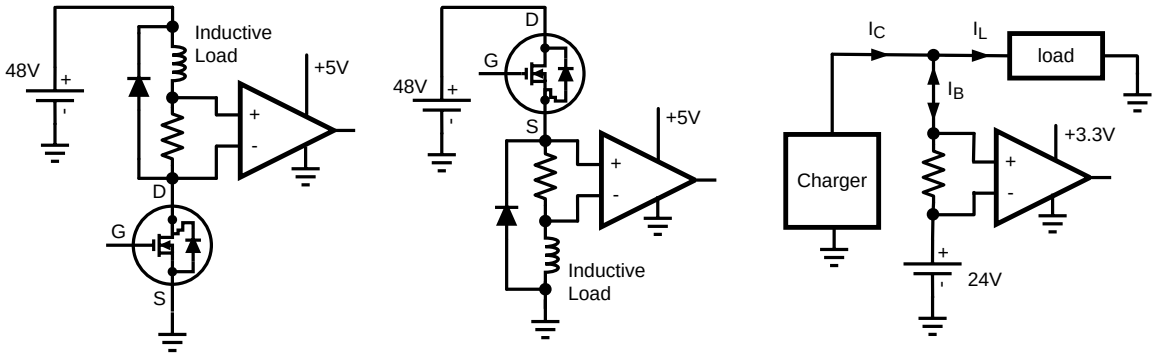
- **High-Side and Low-Side Driver Configuration Current Sensing**
- **Bidirectional Current Measurement**
- **Current Loop to Voltage Conversion**
- **Automotive Fuel Injection Control**
- **Transmission Control**
- **Power Steering**
- **Battery Management Systems**

DESCRIPTION

The LMP8601 and LMP8601Q are fixed 20x gain precision amplifiers. The part will amplify and filter small differential signals in the presence of high common mode voltages. The input common mode voltage range is –22V to +60V when operating from a single 5V supply. With 3.3V supply, the input common mode voltage range is from –4V to +27V. The LMP8601 and LMP8601Q are members of the Linear Monolithic Precision (LMP®) family and are ideal parts for unidirectional and bidirectional current sensing applications. All parameter values of the part that are shown in the tables are 100% tested and all bold values are also 100% tested over temperature.

The part has a precise gain of 20x which is adequate in most targeted applications to drive an ADC to its full scale value. The fixed gain is achieved in two separate stages, a preamplifier with a gain of 10x and an output stage buffer amplifier with a gain of 2x. The connection between the two stages of the signal path is brought out on two pins to enable the possibility to create an additional filter network around the output buffer amplifier. These pins can also be used for alternative configurations with different gain as described in Application Information.

Typical Applications



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DESCRIPTION (CONTINUED)

The mid-rail offset adjustment pin enables the user to use these devices for bidirectional single supply voltage current sensing. The output signal is bidirectional and mid-rail referenced when this pin is connected to the positive supply rail. With the offset pin connected to ground, the output signal is unidirectional and ground-referenced .

The LMP8601Q incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

ESD Tolerance (2), Human Body	For input pins only	±4000V
	For all other pins	±2000V
Machine Model		200V
Charge Device Model		1000V
Supply Voltage (V_S - GND)		6.0V
Continuous Input Voltage ((-IN and +IN)		-22V to 60V
Transient (400 ms)		-25V to 65V
Maximum Voltage at A1, A2, OFFSET and OUT Pins		V_S +0.3V and GND -0.3V
Storage Temperature Range		-65°C to 150°C
Junction Temperature (3)		150°C
Mounting Temperature	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead (10 sec)	260°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) Human Body Model per MIL-STD-883, Method 3015.7. Machine Model, per JESD22-A115-A. Field-Induced Charge-Device Model, per JESD22-C101-C.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

Operating Ratings (1)

Supply Voltage (V_S – GND)		3.0V to 5.5V
Offset Voltage (Pin 7)		0 to V_S
Temperature Range (2)	Packaged devices	-40°C to +125°C
Package Thermal Resistance (2)	8-Pin SOIC (θ_{JA})	190°C/W

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

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3.3V Electrical Characteristics (1)

Unless otherwise specified, all limits ensured at T_A = 25°C, V_S = 3.3V, GND = 0V, -4V ≤ V_{CM} ≤ 27V, and R_L = ∞, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		Min (2)	Typ (3)	Max (2)	Unit
Overall Performance (From -IN (pin 1) and +IN (pin 8) to OUT (pin 5) with pins A1 (pin 3) and A2 (pin 4) connected)							
I_S	Supply Current			**0.6**	1	**1.3**	mA
A_V	Total Gain			19.9	20	20.1	V/V
	Gain Drift (4)	-40°C ≤ T_A ≤ 125°C			-2.7	**±20**	ppm/°C
SR	Slew Rate (5)	V_{IN} = ±0.165V		0.4	0.7		V/µs
BW	Bandwidth			50	60		kHz
V_{OS}	Input Offset Voltage	V_{CM} = V_S / 2			0.15	±1	mV
TCV_{OS}	Input Offset Voltage Drift (6)	-40°C ≤ T_A ≤ 125°C			2	**±10**	µV/°C
e_n	Input Referred Voltage Noise	0.1 Hz - 10 Hz, 6 Sigma			16.4		μV_{P-P}
		Spectral Density, 1 kHz			830		$nV/\sqrt{Hz}$
PSRR	Power Supply Rejection Ratio	DC, 3.0V ≤ V_S ≤ 3.6V, V_{CM} = V_S/2		**70**	86		dB
	Mid-scale Offset Scaling Accuracy				±0.15	±0.5	%
		Input Referred				±0.413	mV
Preamplifier (From input pins -IN (pin 1) and +IN (pin 8) to A1 (pin 3))							
R_{CM}	Input Impedance Common Mode	-4V ≤ V_{CM} ≤ 27V		**250**	295	**350**	kΩ
R_{DM}	Input Impedance Differential Mode	-4V ≤ V_{CM} ≤ 27V		**500**	590	**700**	kΩ
V_{OS}	Input Offset Voltage	V_{CM} = V_S / 2			±0.15	±1	mV
DC CMRR	DC Common Mode Rejection Ratio	-2V ≤ V_{CM} ≤ 24V		**86**	96		dB
AC CMRR	AC Common Mode Rejection Ratio (7)	f = 1 kHz		80	94		dB
		f = 10 kHz			85		
CMVR	Input Common Mode Voltage Range	for 80 dB CMRR		**-4**		**27**	V
$A1_V$	Gain (4)			9.95	10.0	10.05	V/V
R_{F-INT}	Output Impedance Filter Resistor			**99**	100	**101**	kΩ
TCR_{F-INT}	Output Impedance Filter Resistor Drift				±5	**±50**	ppm/°C
A1 V_{OUT}	A1 Output Voltage Swing	V_{OL}	R_L = ∞		2	**10**	mV
		V_{OH}		**3.2**	3.25		V
Output Buffer (From A2 (pin 4) to OUT(pin 5))							
V_{OS}	Input Offset Voltage	0V ≤ V_{CM} ≤ V_S		-2 **-2.5**	±0.5	2 **2.5**	mV
$A2_V$	Gain (4)			1.99	2	2.01	V/V
I_B	Input Bias Current of A2 (8),				-40		fA
						±20	nA
A2 V_{OUT}	A2 Output Voltage Swing (9) (10)	V_{OL}	R_L = 100 kΩ		4	**20**	mV
		V_{OH}		**3.28**	3.29		V

(1) The electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Datasheet min/max specification limits are ensured by test.
(3) Typical values represent the most likely parameter norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) Both the gain of the preamplifier $A1_V$ and the gain of the buffer amplifier $A2_V$ are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits
(5) Slew rate is the average of the rising and falling slew rates.
(6) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(7) AC Common Mode Signal is a $5V_{PP}$ sine-wave (0V to 5V) at the given frequency.
(8) Positive current corresponds to current flowing into the device
(9) For this test input is driven from A1 stage.
(10) For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.

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3.3V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits ensured at T_A = 25°C, V_S = 3.3V, GND = 0V, -4V ≤ V_{CM} ≤ 27V, and R_L = ∞, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min(2)	Typ(3)	Max(2)	Unit
I_{SC}	Output Short-Circuit Current (11)	Sourcing, V_{IN} = V_S, V_{OUT} = GND	-25	-38	-60	mA
		Sinking, V_{IN} = GND, V_{OUT} = V_S	30	46	65	

(11) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

5V Electrical Characteristics (1)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, -22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		Min(2)	Typ(3)	Max(2)	Unit
Overall Performance (From -IN (pin 1) and +IN (pin 8) to OUT (pin 5) with pins A1 (pin 3) and A2 (pin 4) connected)							
I_S	Supply Current			**0.7**	1.1	**1.5**	mA
A_V	Total Gain (4)			19.9	20	20.1	V/V
	Gain Drift	-40°C ≤ T_A ≤ 125°C			-2.8	**±20**	ppm/°C
SR	Slew Rate (5)	V_{IN} = ±0.25V		0.6	0.83		V/µs
BW	Bandwidth			50	60		kHz
V_{OS}	Input Offset Voltage				0.15	±1	mV
TCV_{OS}	Input Offset Voltage Drift (6)	-40°C ≤ T_A ≤ 125°C			2	**±10**	µV/°C
e_N	Input Referred Voltage Noise	0.1 Hz - 10 Hz, 6 Sigma			17.5		μV_{P-P}
		Spectral Density, 1 kHz			890		$nV/\sqrt{Hz}$
PSRR	Power Supply Rejection Ratio	DC 4.5V ≤ V_S ≤ 5.5V		**70**	90		dB
	Mid-scale Offset Scaling Accuracy				±0.15	±0.5	%
		Input Referred				±0.625	mV
Preamplifier (From input pins -IN (pin 1) and +IN (pin 8) to A1 (pin 3))							
R_{CM}	Input Impedance Common Mode	0V ≤ V_{CM} ≤ 60V		**250**	295	**350**	kΩ
		-20V ≤ V_{CM} ≤ 0V		**165**	193	**250**	kΩ
R_{DM}	Input Impedance Differential Mode	0V ≤ V_{CM} ≤ 60V		**500**	590	**700**	kΩ
		-20V ≤ V_{CM} ≤ 0V		**300**	386	**500**	kΩ
V_{OS}	Input Offset Voltage	V_{CM} = V_S / 2			±0.15	±1	mV
DC CMRR	DC Common Mode Rejection Ratio	-20V ≤ V_{CM} ≤ 60V		**90**	105		dB
AC CMRR	AC Common Mode Rejection Ratio (7)	f = 1 kHz		80	96		dB
		f = 10 kHz			83		
CMVR	Input Common Mode Voltage Range	for 80 dB CMRR		**-22**		**60**	V
$A1_V$	Gain (4)			9.95	10	10.05	V/V
R_{F-INT}	Output Impedance Filter Resistor			**99**	100	**101**	kΩ
TCR_{F-INT}	Output Impedance Filter Resistor Drift				±5	**±50**	ppm/°C
A1 V_{OUT}	A1 Ouput Voltage Swing	V_{OL}	R_L = ∞		2	**10**	mV
		V_{OH}		**4.95**	4.985		V

(1) The electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Datasheet min/max specification limits are ensured by test.
(3) Typical values represent the most likely parameter norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) Both the gain of the preamplifier $A1_V$ and the gain of the buffer amplifier $A2_V$ are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits
(5) Slew rate is the average of the rising and falling slew rates.
(6) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(7) AC Common Mode Signal is a $5V_{PP}$ sine-wave (0V to 5V) at the given frequency.

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5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, -22V ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		Min (2)	Typ (3)	Max (2)	Unit
Output Buffer (From A2 (pin 4) to OUT(pin 5))							
V_{OS}	Input Offset Voltage	0V ≤ V_{CM} ≤ V_S		-2 **-2.5**	±0.5	2 **2.5**	mV
$A2_V$	Gain (8)			1.99	2	2.01	V/V
I_B	Input Bias Current of A2 (9)				-40		fA
						±20	nA
A2 V_{OUT}	A2 Ouput Voltage Swing (10) (11)	V_{OL}	R_L = 100 kΩ		4	**20**	mV
		V_{OH}		**4.98**	4.99		V
I_{SC}	Output Short-Circuit Current (12)	Sourcing, V_{IN} = V_S, V_{OUT} = GND		–25	–42	–60	mA
		Sinking, V_{IN} = GND, V_{OUT} = V_S		30	48	65	

(8) Both the gain of the preamplifier $A1_V$ and the gain of the buffer amplifier $A2_V$ are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits
(9) Positive current corresponds to current flowing into the device
(10) For this test input is driven from A1 stage.
(11) For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.
(12) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

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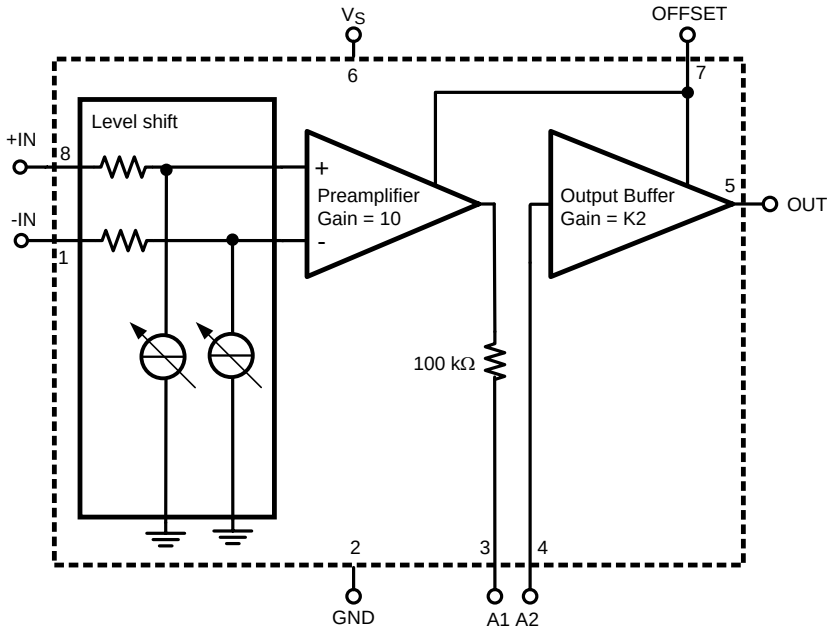
DEVICE INFORMATION

Block Diagram



K2 = 2

Figure 1. Block Diagram

Connection Diagram

Top View

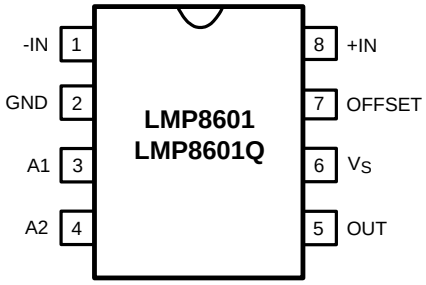


Figure 2. 8-Pin SOIC Package
see package number D0008A

Table 1. Pin Descriptions

Name	Pin No.		Description
GND	2	Power Supply	Power Ground
V_S	6		Positive Supply Voltage
-IN	1	Inputs	Negative Input
+IN	8		Positive Input
A1	3	Filter Network	Preamplifier output
A2	4		Input from the external filter network and / or A1
OFFSET	7	Offset	DC Offset for bidirectional signals

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Table 1. Pin Descriptions (continued)

Name	Pin No.		Description
OUT	5	Output	Single ended output

Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard. Automotive Grade products are identified with the letter Q. Fully compliant PPAP documentation is available. For more information go to http://www.ti.com/lsds/ti/apps/automotive/end_equipment.page.

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Typical Performance Characteristics

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, -22 ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

V_{OS} vs. V_{CM} at V_S = 3.3V

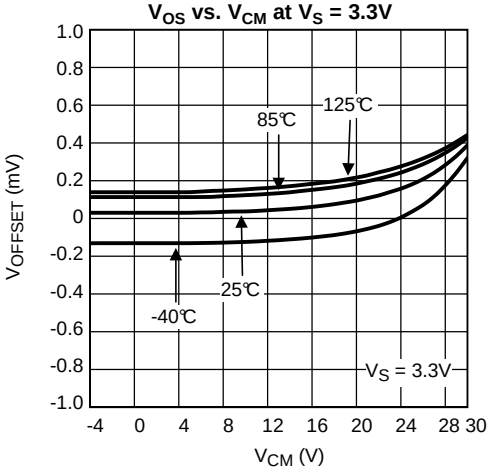

Figure 3.

V_{OS} vs. V_{CM} at V_S = 5V

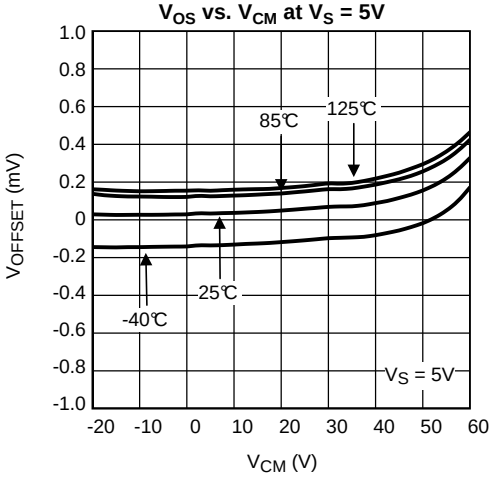

Figure 4.

Input Bias Current Over Temperature (+IN and -IN pins) at V_S = 3.3V

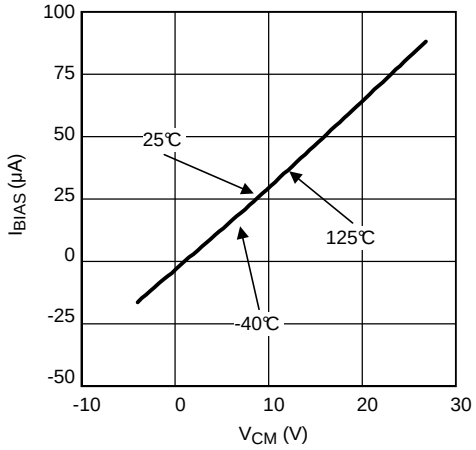

Figure 5.

Input Bias Current Over Temperature (+IN and -IN pins) at V_S = 5V

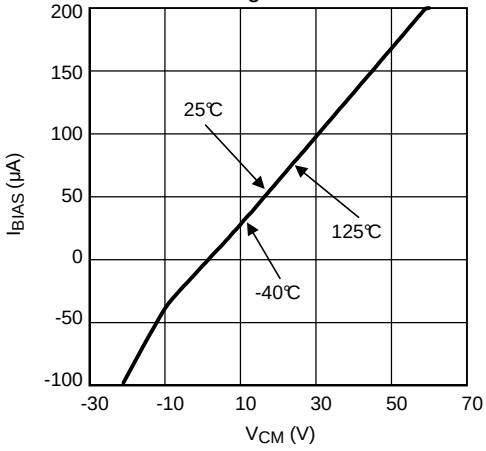

Figure 6.

Input Bias Current Over Temperature (A2 pin) at V_S = 5V

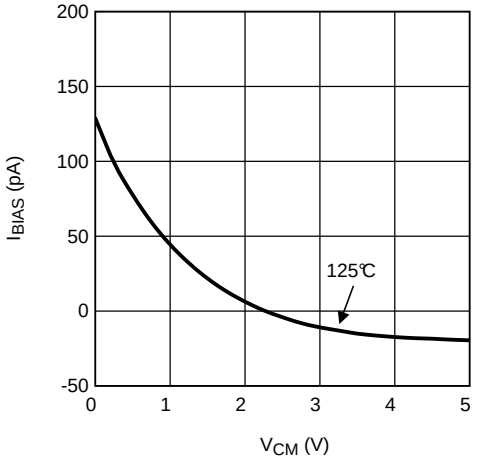

Figure 7.

Input Bias Current Over Temperature (A2 pin) at V_S = 5V

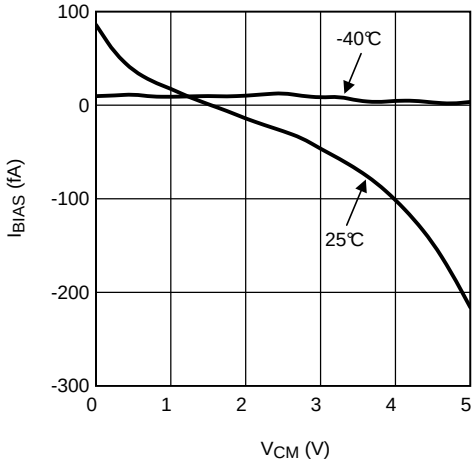

Figure 8.

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Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, -22 ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Input Referred Voltage Noise vs. Frequency

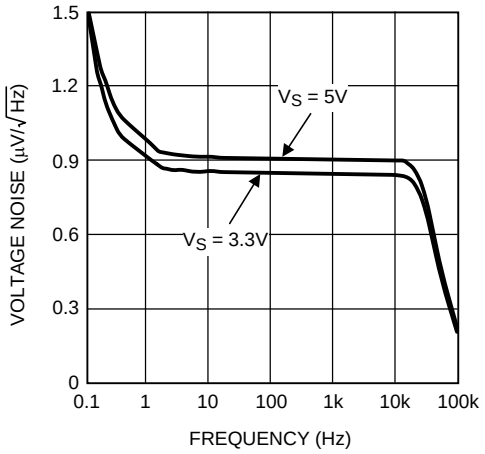

Figure 9.

PSRR vs. Frequency

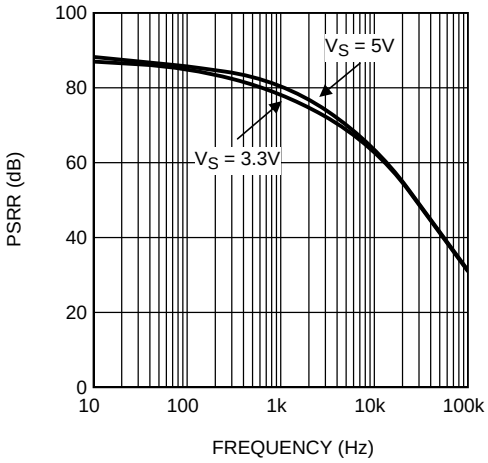

Figure 10.

Gain vs. Frequency at V_S = 3.3V

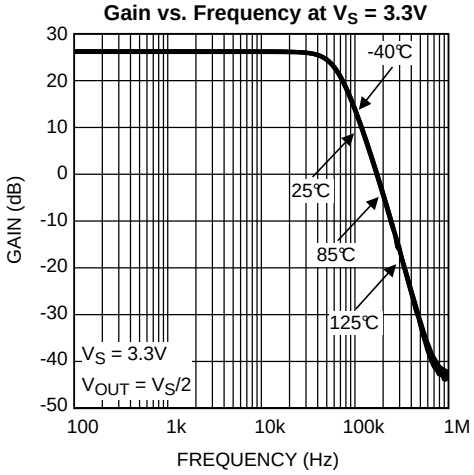

Figure 11.

Gain vs. Frequency at V_S = 5V

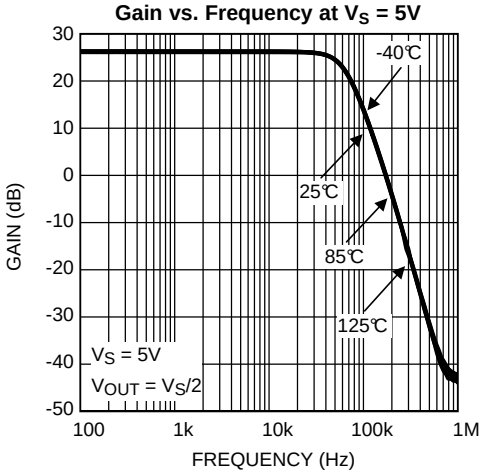

Figure 12.

CMRR vs. Frequency at V_S = 3.3V

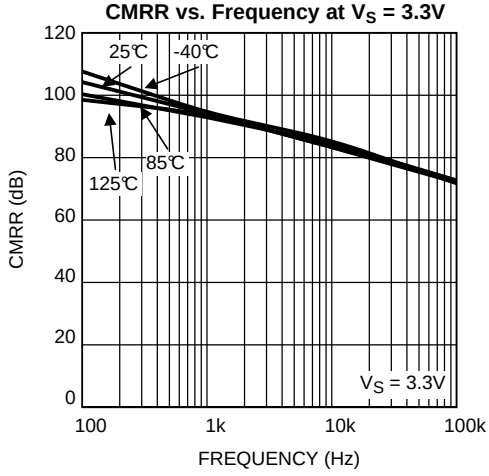

Figure 13.

CMRR vs. Frequency at V_S = 5V

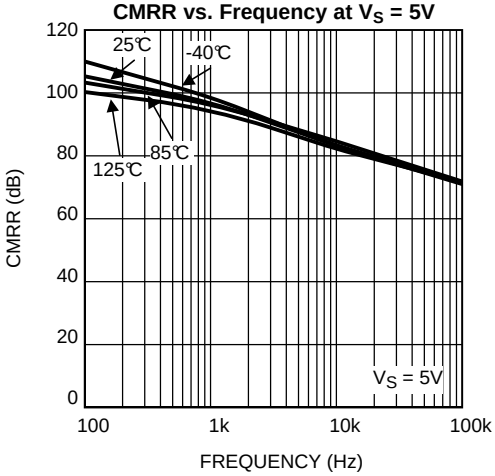

Figure 14.

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Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, -22 ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Step Response at V_S = 3.3V

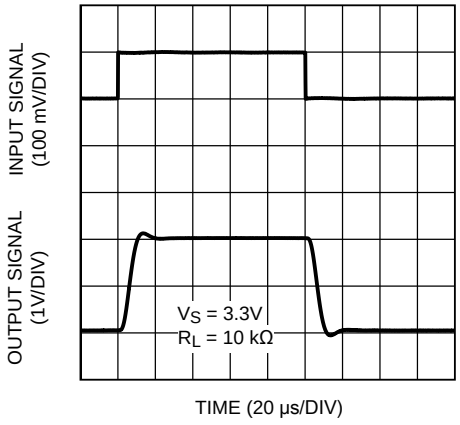

Figure 15.

Step Response at V_S = 5V

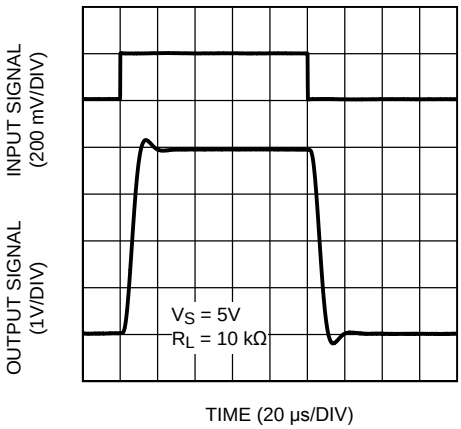

Figure 16.

Settling Time (Falling Edge) at V_S = 3.3V

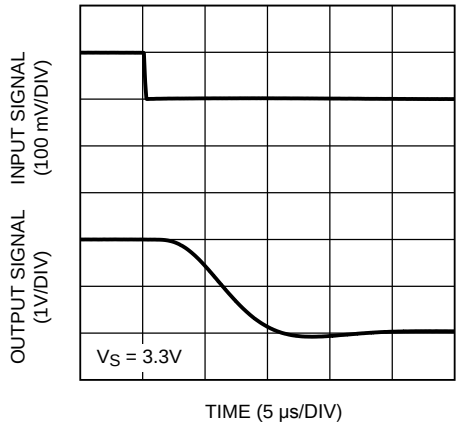

Figure 17.

Settling Time (Falling Edge) at V_S = 5V

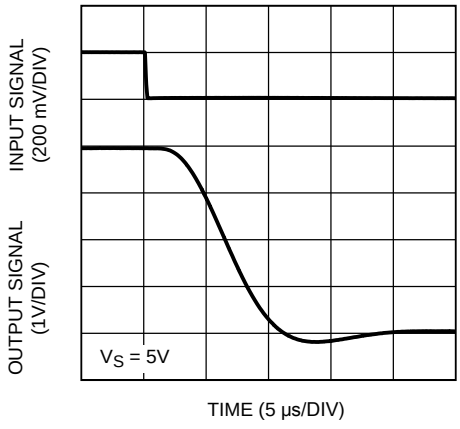

Figure 18.

Settling Time (Rising Edge) at V_S = 3.3V

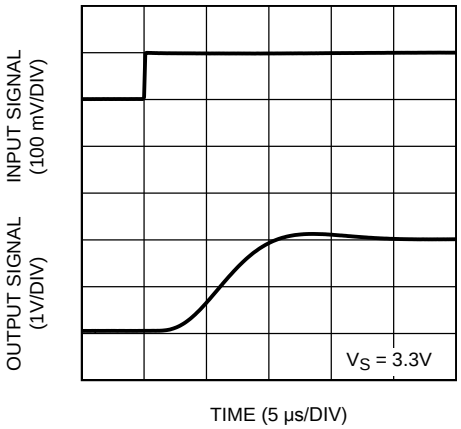

Figure 19.

Settling Time (Rising Edge) at V_S = 5V

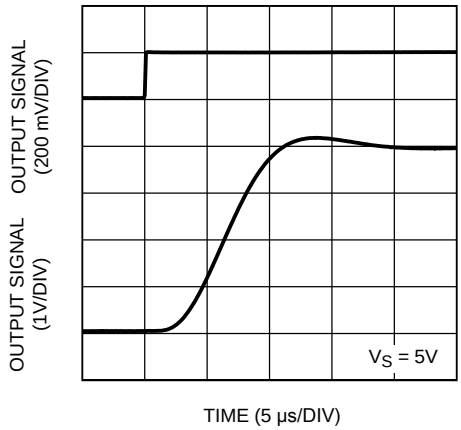

Figure 20.

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Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, -22 ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Positive Swing vs. R_{LOAD} at V_S = 3.3V

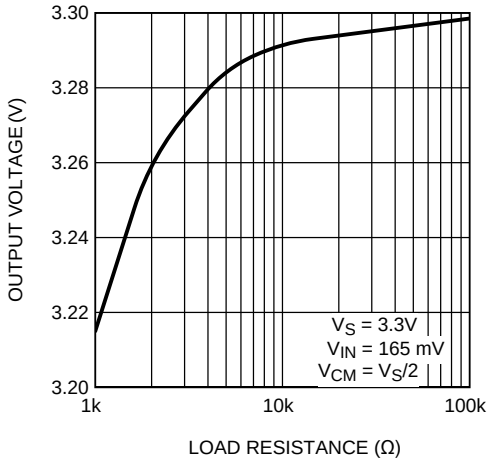

Figure 21.

Negative Swing vs. R_{LOAD} at V_S = 3.3V

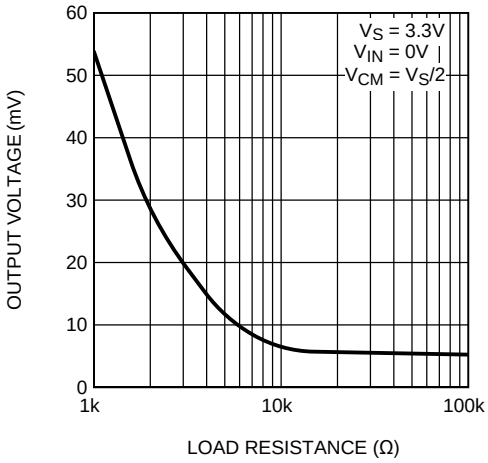

Figure 22.

Positive Swing vs. R_{LOAD} V_S = 5V

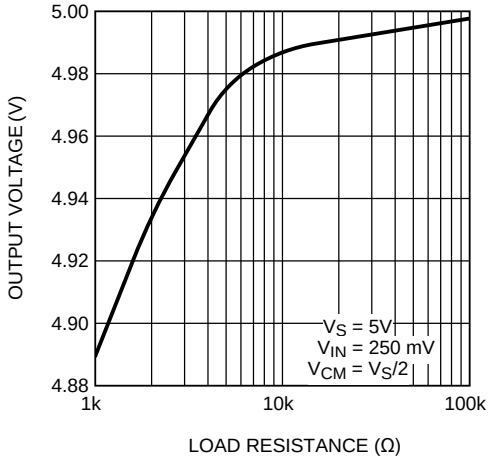

Figure 23.

Negative Swing vs. R_{LOAD} at V_S = 5V

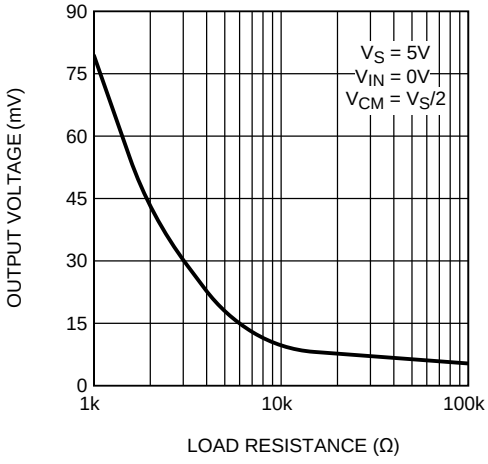

Figure 24.

V_{OS} Distribution at V_S = 3.3V

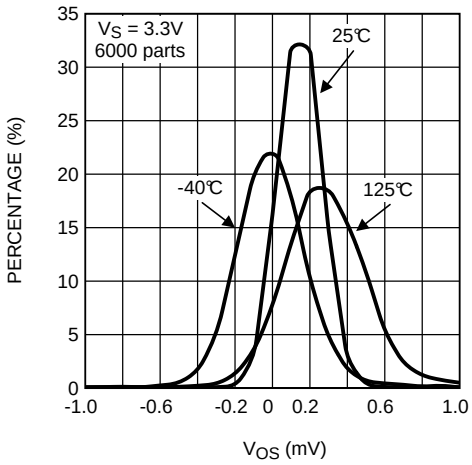

Figure 25.

V_{OS} Distribution at V_S = 5V

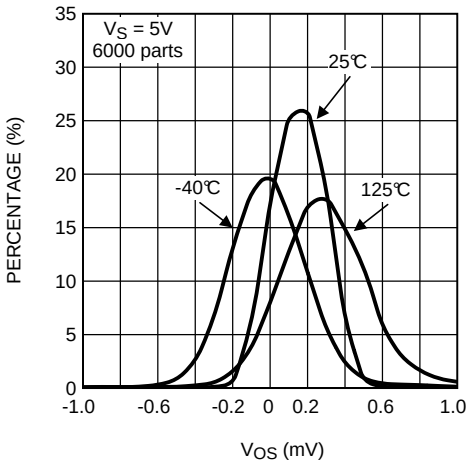

Figure 26.

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Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, -22 ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

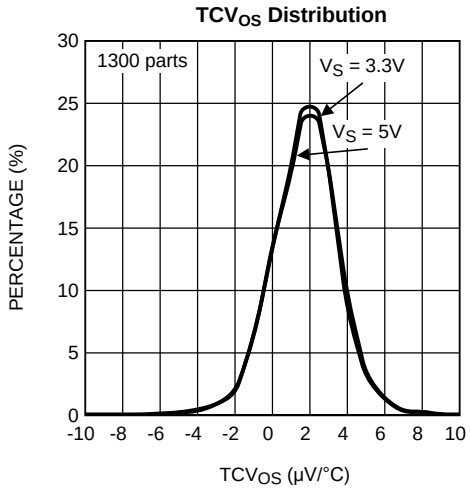

Figure 27.

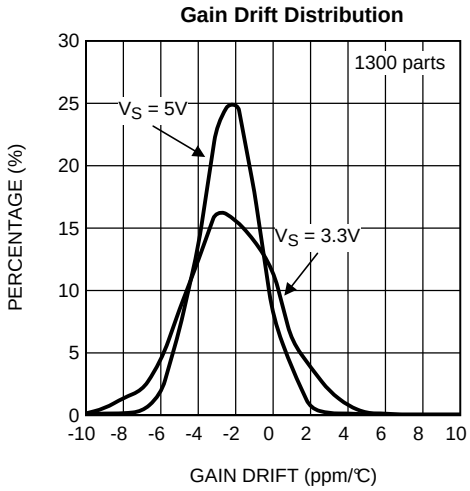

Figure 28.

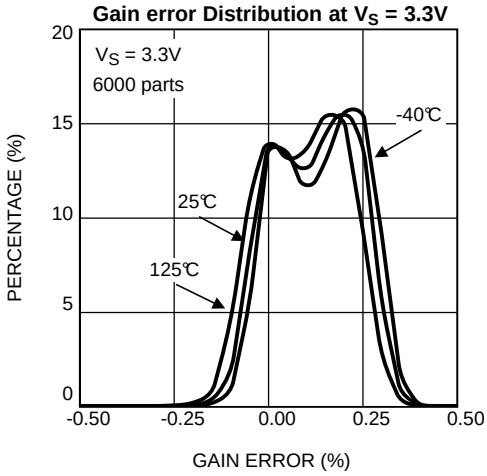

Figure 29.

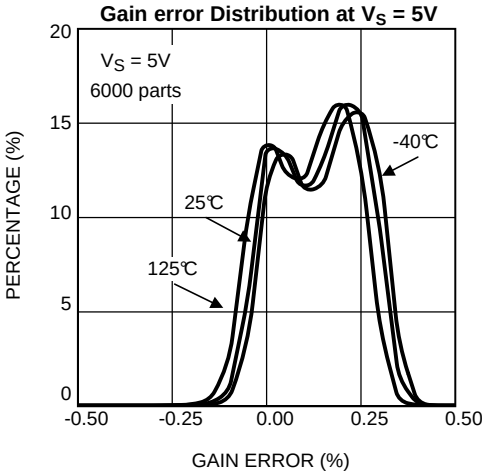

Figure 30.

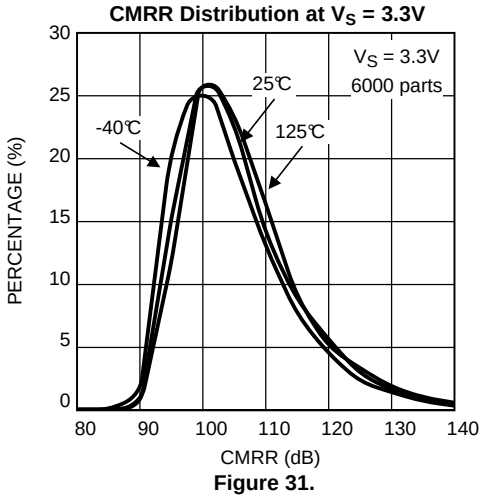

Figure 31.

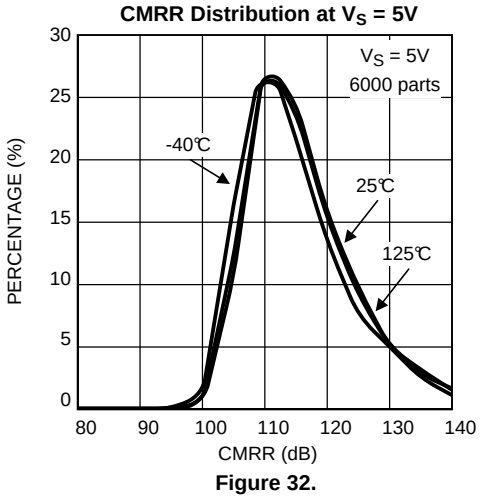

Figure 32.

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Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5V, GND = 0V, -22 ≤ V_{CM} ≤ 60V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10nF between V_S and GND.

Output Voltage vs. VIN

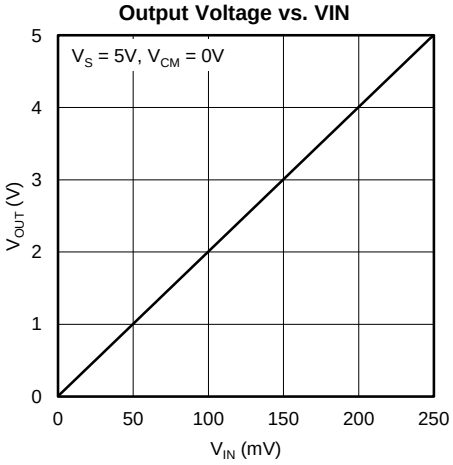

Figure 33.

Output Voltage vs. VIN (Zoom close to 0V)

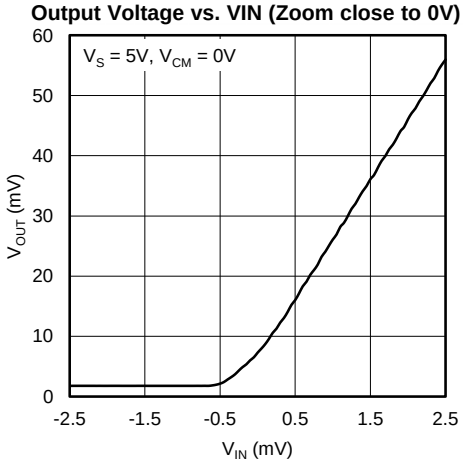

Figure 34.

Output Voltage vs. VIN

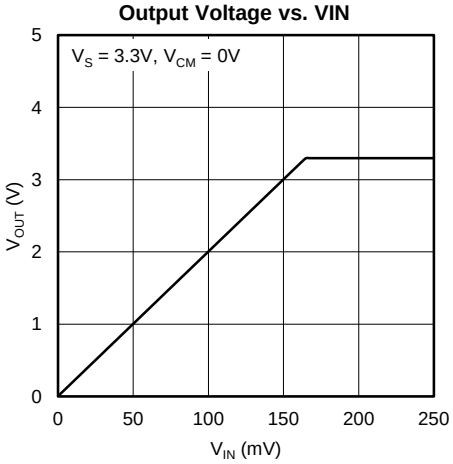

Figure 35.

Output Voltage vs. VIN (Zoom close to 0V)

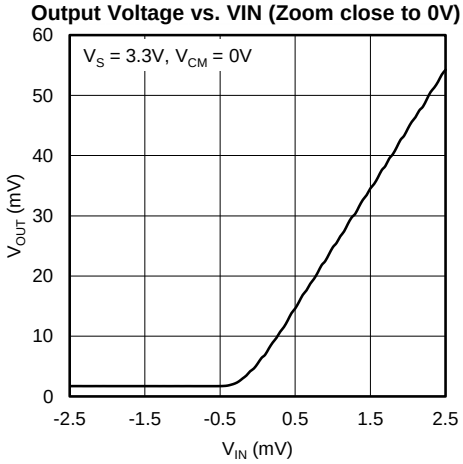

Figure 36.

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APPLICATION INFORMATION

GENERAL

The LMP8601 and LMP8601Q are fixed gain differential voltage precision amplifiers with a gain of 20x and a -22V to +60V input common mode voltage range when operating from a single 5V supply or a -4V to +27V input common mode voltage range when operating from a single 3.3V supply. The LMP8601 and LMP8601Q are members of the LMP family and are ideal parts for unidirectional and bidirectional current sensing applications. Because of the proprietary chopping level-shift input stage the LMP8601/LMP8601Q achieve very low offset, very low thermal offset drift, and very high CMRR. The LMP8601 and LMP8601Q will amplify and filter small differential signals in the presence of high common mode voltages.

The LMP8601/LMP8601Q use level shift resistors at the inputs. Because of these resistors, the LMP8601/LMP8601Q can easily withstand very large differential input voltages that may exist in fault conditions where some other less protected high-performance current sense amplifiers might sustain permanent damage.

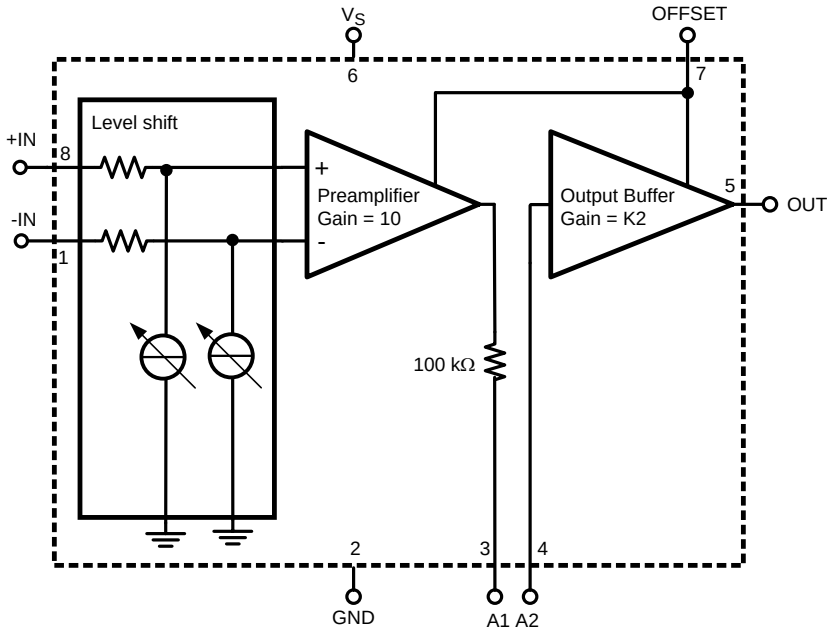
PERFORMANCE GUARANTIES

To guaranty the high performance of the LMP8601/ LMP8601Q, all minimum and maximum values shown in the parameter tables of this data sheet are 100% tested where all bold limits are also 100% tested over temperature.

THEORY OF OPERATION

The schematic shown in Figure 37 gives a schematic representation of the internal operation of the LMP8601/LMP8601Q.

The signal on the input pins is typically a small differential voltage across a current sensing shunt resistor. The input signal may appear at a high common mode voltage. The input signals are accessed through two input resistors. The proprietary chopping level-shift current circuit pulls or pushes current through the input resistors to bring the common mode voltage behind these resistors within the supply rails. Subsequently, the signal is gained up by a factor of 10 and brought out on the A1 pin through a trimmed 100 kΩ resistor. In the application, additional gain adjustment or filtering components can be added between the A1 and A2 pins as will be explained in subsequent sections. The signal on the A2 pin is further amplified by a factor of 2 and brought out on the OUT pin. The OFFSET pin allows the output signal to be level-shifted to enable bidirectional current sensing as will be explained below.



K2 = 2

Figure 37. Theory of Operation

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ADDITIONAL SECOND ORDER LOW PASS FILTER

The LMP8601/LMP8601Q has a third order Butterworth low-pass characteristic with a typical bandwidth of 60 kHz integrated in the preamplifier stage of the part. The bandwidth of the output buffer can be reduced by adding a capacitor on the A1 pin to create a first order low pass filter with a time constant determined by the 100 kΩ internal resistor and the external filter capacitor.

It is also possible to create an additional second order Sallen-Key low pass filter by adding external components R_2, C_1 and C_2. Together with the internal 100 kΩ resistor R_1 as illustrated in Figure 38, this circuit creates a second order low-pass filter characteristic.

When the corner frequency of the additional filter is much lower than 60 kHz, the transfer function of the described amplifier van be written as:

$$H(s) = \frac{K_1 * K_2 \dfrac{1}{R_1R_2C_1C_2}}{s^2 + s * \left[\dfrac{1}{R_1C_2} + \dfrac{1}{R_2C_2} + \dfrac{(1 - K_2)}{R_2C_1}\right] + \dfrac{1}{R_1R_2C_1C_2}} \quad (1)$$

Where K_1 equals the gain of the preamplifier and K_2 that of the buffer amplifier.

Equation 1 can be written in the normalized frequency response for a 2nd order low pass filter:

$$G(j\omega) = K_1 * \frac{K_2}{\dfrac{(j\omega)^2}{\omega_o^2} + \dfrac{j\omega}{Q\omega_o} + 1} \quad (2)$$

The cutoff frequency ω_o in rad/sec (divide by 2π to get the cut-off frequency in Hz) is given by:

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (3)$$

and the quality factor of the filter is given by:

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 + (1 - K_2) * R_1C_2} \quad (4)$$

With K_2 = 2x, Equation 4 transforms results in:

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 - R_1C_2} \quad (5)$$

With this filter gain K2= 2x, the design procedure can be very simple if the two capacitors are chosen to be equal, C_1=C_2=C. In this case, given the predetermined value of R1 = 100kΩ(the internal resistor), the quality factor is set solely by the value of the resistor R_2.

R_2 can be calculated based on the desired value of Q as the first step of the design procedure with Equation 6:

$$R_2 = \frac{R_1}{Q^2} \quad (6)$$

For instance, the value of Q can be set to 0.5√2 to create a Butterworth response, to 1/√3 to create a Bessel response, or a 0.5 to create a critically damped response. Once the value of R_2 has been found, the second and last step of the design procedure is to calculate the required value of C to give the desired low-pass cut-off frequency using:

$$C = \frac{Q}{R_1\omega_o} \quad (7)$$

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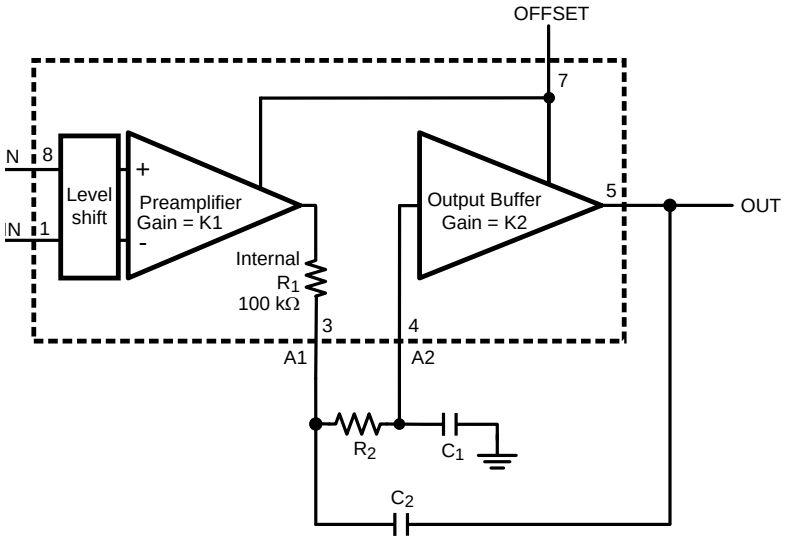
Note that the frequency response achieved using this procedure will only be accurate if the cut-off frequency of the second order filter is much smaller than the intrinsic 60 kHz low-pass filter. In other words, to have the frequency response of the LMP8601/LMP8601Q circuit chosen such that the internal poles do not affect the external second order filter.



K1 = 10, K2 = 2

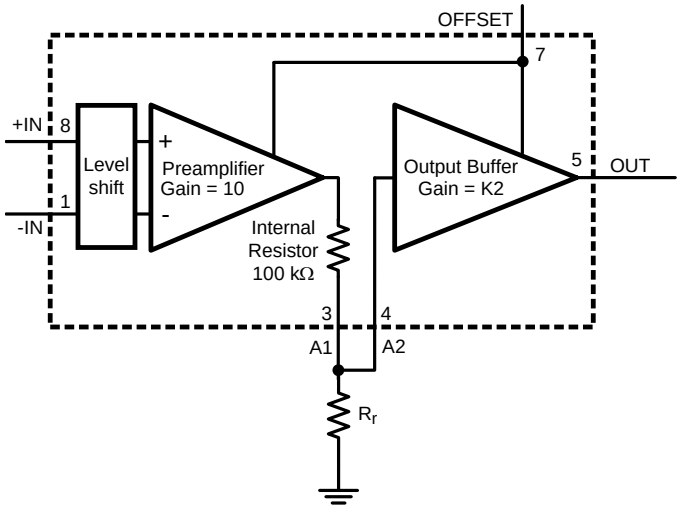
Figure 38. Second Order Low Pass Filter

GAIN ADJUSTMENT

The gain of the LMP8601/LMP8601Q is 20; however, this gain can be adjusted as the signal path in between the two internal amplifiers is available on the external pins.

Reduce Gain

Figure 39 shows the configuration that can be used to reduce the gain of the LMP8601/LMP8601Q.



K2 = 2

Figure 39. Reduce Gain

R_r creates a resistive divider together with the internal 100 kΩ resistor such that the reduced gain G_r becomes:

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$$G_r = \frac{20\ R_r}{R_r + 100\ k\Omega} \tag{8}$$

Given a desired value of the reduced gain G_r, using this equation the required value for R_r can be calculated with:

$$R_r = 100\ k\Omega\ X\ \frac{G_r}{20 - G_r} \tag{9}$$

Increase Gain

Figure 40 shows the configuration that can be used to increase the gain of the LMP8601/LMP8601Q.

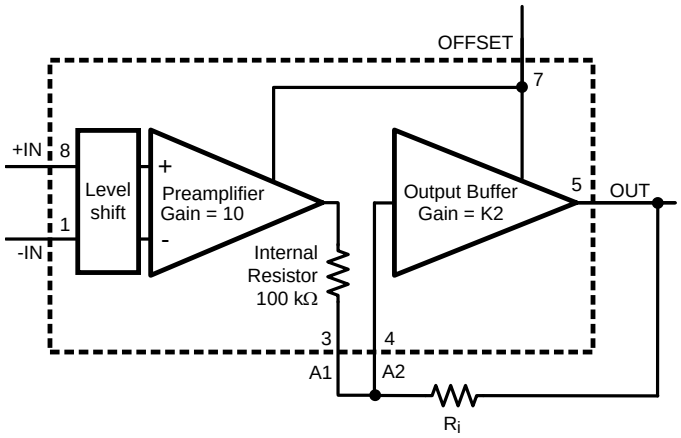
R_i creates positive feedback from the output pin to the input of the buffer amplifier. The positive feedback increases the gain. The increased gain G_i becomes:

$$G_i = \frac{20\ R_i}{R_i - 100\ k\Omega} \tag{10}$$

From this equation, for a desired value of the gain, the required value of R_i can be calculated with:

$$R_i = 100\ k\Omega\ X\ \frac{G_i}{G_i - 20} \tag{11}$$

It should be noted from the equation for the gain G_i that for large gains R_i approaches 100 kΩ. In this case, the denominator in the equation becomes close to zero. In practice, for large gains the denominator will be determined by tolerances in the value of the external resistor R_i and the internal 100 kΩ resistor. In this case, the gain becomes very inaccurate. If the denominator becomes equal to zero, the system will even become instable. It is recommended to limit the application of this technique to gain values of 50 or smaller.



K2 = 2

Figure 40. Increase Gain

BIDIRECTIONAL CURRENT SENSING

The signal on the A1 and OUT pins is ground-referenced when the OFFSET pin is connected to ground. This means that the output signal can only represent positive values of the current through the shunt resistor, so only currents flowing in one direction can be measured. When the offset pin is tied to the positive supply rail, the signal on the A1 and OUT pins is referenced to a mid-rail voltage which allows bidirectional current sensing. When the offset pin is connected to a voltage source, the output signal will be level shifted to that voltage divided by two. In principle, the output signal can be shifted to any voltage between 0 and $V_S/2$ by applying twice that voltage to the OFFSET pin.

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With the offset pin connected to the supply pin (V_S) the operation of the amplifier will be fully bidirectional and symmetrical around 0V differential at the input pins. The signal at the output will follow this voltage difference multiplied by the gain and at an offset voltage at the output of half V_S.

Example:

With 5V supply and a gain of 20x, a differential input signal of +10mV will result in 2.7V at the output pin. similarly -10mV at the input will result in 2.3V at the output pin.

NOTE

The OFFSET pin has to be driven from a very low-impedance source (<10Ω). This is because the OFFSET pin internally connects directly to the resistive feedback networks of the two gain stages. When the OFFSET pin is driven from a relatively large impedance (e.g. a resistive divider between the supply rails) accuracy will decrease.

POWER SUPPLY DECOUPLING

In order to decouple the LMP8601/LMP8601Q from AC noise on the power supply, it is recommended to use a 0.1 µF bypass capacitor between the V_S and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases an additional 10 µF bypass capacitor may further reduce the supply noise.

DRIVING SWITCHED CAPACITIVE LOADS

Some ADCs load their signal source with a sample and hold capacitor. The capacitor may be discharged prior to being connected to the signal source. If the LMP8601/LMP8601Q is driving such ADCs the sudden current that should be delivered when the sampling occurs may disturb the output signal. This effect was simulated with the circuit shown in Figure 41 where the output is to a capacitor that is driven by a rail to rail square wave.

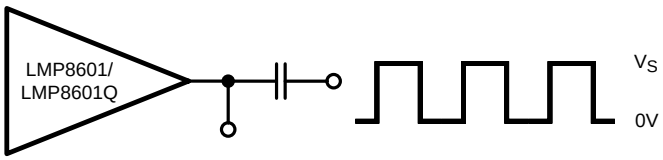

Figure 41. Driving Switched Capacitive Load

This circuit simulates the switched connection of a discharged capacitor to the LMP8601/LMP8601Q output. The resulting V_{OUT} disturbance signals are shown in Figure 42 andFigure 43.

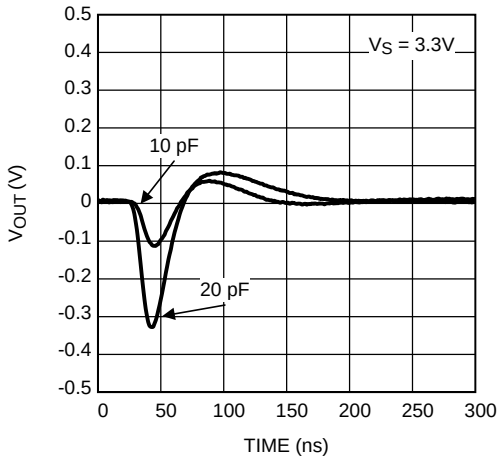

Figure 42. Capacitive Load Response at 3.3V

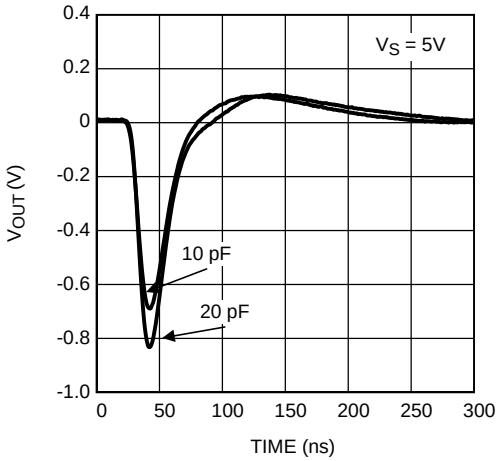

Figure 43. Capacitive Load Response at 5.0V

These figures can be used to estimate the disturbance that will be caused when driving a switched capacitive load. To minimize the error signal introduced by the sampling that occurs on the ADC input, an additional RC filter can be placed in between the LMP8601/LMP8601Q and the ADC as illustrated in Figure 44.

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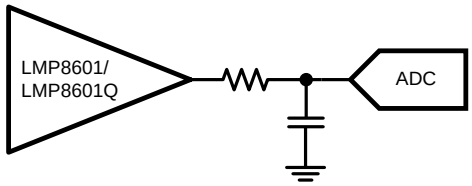
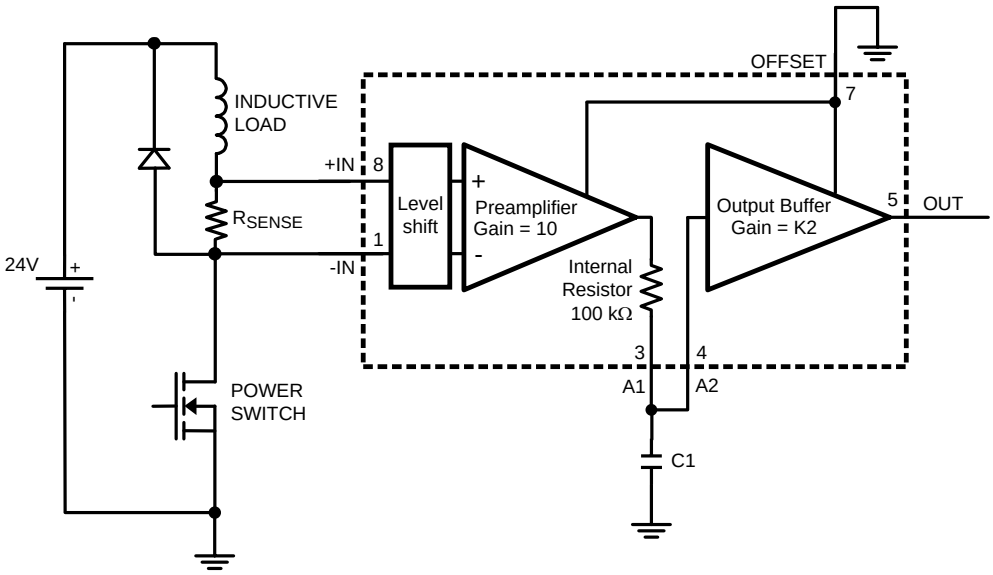


Figure 44. Reduce Error When Driving ADCs

The external capacitor absorbs the charge that flows when the ADC sampling capacitor is connected. The external capacitor should be much larger than the sample and hold capacitor at the input of the ADC and the RC time constant of the external filter should be such that the speed of the system is not affected.

LOW SIDE CURRENT SENSING APPLICATION

Figure 45 illustrates a low side current sensing application with a low side driver. The power transistor is pulse width modulated to control the average current flowing through the inductive load which is connected to a relatively high battery voltage. The current through the load is measured across a shunt resistor R_{SENSE} in series with the load. When the power transistor is on, current flows from the battery through the inductive load, the shunt resistor and the power transistor to ground. In this case, the common mode voltage on the shunt is close to ground. When the power transistor is off, current flows through the inductive load, through the shunt resistor and through the freewheeling diode. In this case the common mode voltage on the shunt is at least one diode voltage drop above the battery voltage. Therefore, in this application the common mode voltage on the shunt is varying between a large positive voltage and a relatively low voltage. Because the large common mode voltage range of the LMP8601/LMP8601Q and because of the high AC common mode rejection ratio, the LMP8601/LMP8601Q is very well suited for this application.



R_{SENSE} = 0.01Ω, K2 = 2, V_{OUT} = 0.2 V/A

Figure 45. Low Side Current Sensing Application

HIGH SIDE CURRENT SENSING APPLICATION

Figure 46 illustrates the application of the LMP8601/LMP8601Q in a high side sensing application. This application is similar to the low side sensing discussed above, except in this application the common mode voltage on the shunt drops below ground when the driver is switched off. Because the common mode voltage range of the LMP8601/LMP8601Q extends below the negative rail, the LMP8601/LMP8601Q is also very well suited for this application.

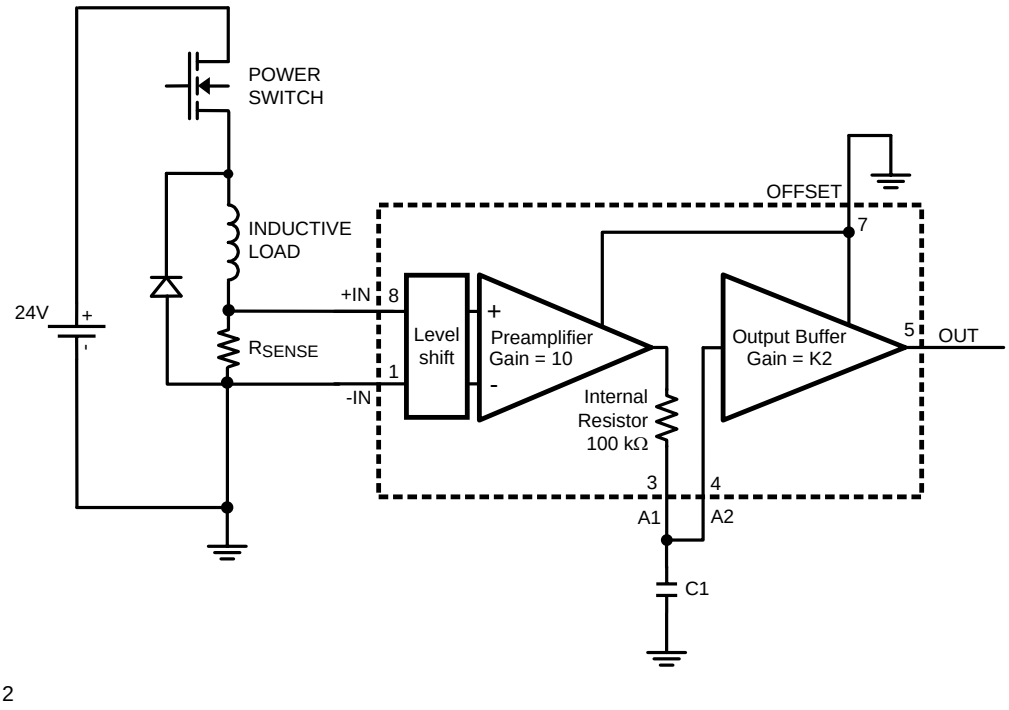


Figure 46. High Side Current Sensing Application

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BATTERY CURRENT MONITOR APPLICATION

This application example shows how the LMP8601/LMP8601Q can be used to monitor the current flowing in and out a battery pack. The fact that the LMP8601/LMP8601Q can measure small voltages at a high offset voltage outside the parts own supply range makes this part a very good choice for such applications. If the load current of the battery is higher then the charging current, the output voltage of the LMP8601/LMP8601Q will be above the “half offset voltage” for a net current flowing out of the battery. When the charging current is higher then the load current the output will be below this “half offset voltage”.

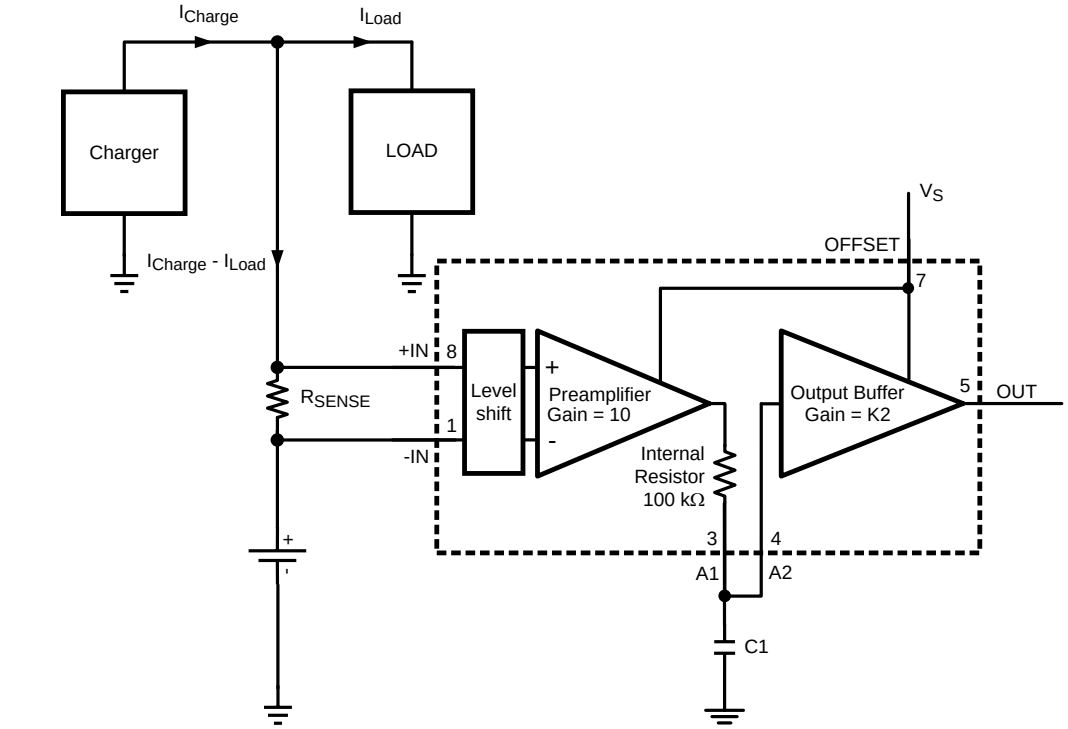

Figure 47. Battery Current Monitor Application

ADVANCED BATTERY CHARGER APPLICATION

The above circuit can be used to realize an advanced battery charger that has the capability to monitor the exact net current that flows in and out the battery as show in Figure 48. The output signal of the LMP8601/LMP8601Q is digitized with the A/D converter and used as an input for the charge controller. The Charge controller can me used to regulate the charger circuit to deliver exactly the current that is required by the load, avoiding overcharging a fully loaded battery

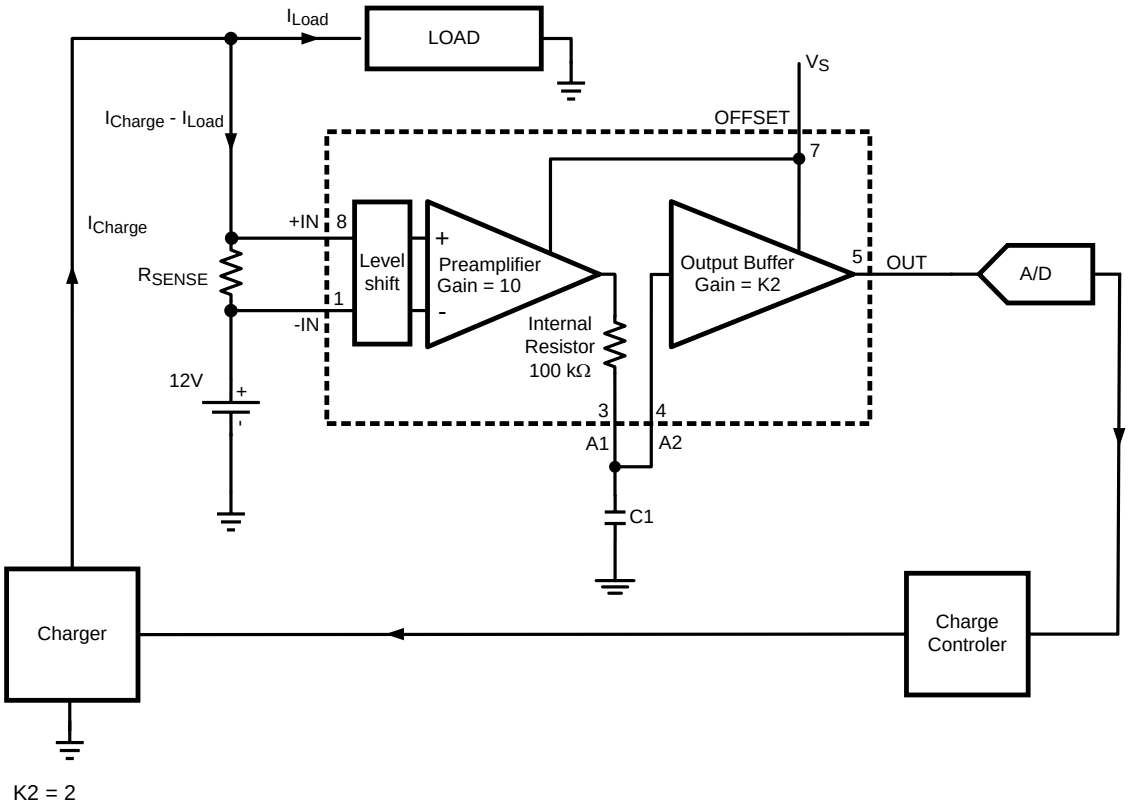

Figure 48. Advanced Battery Charger Application

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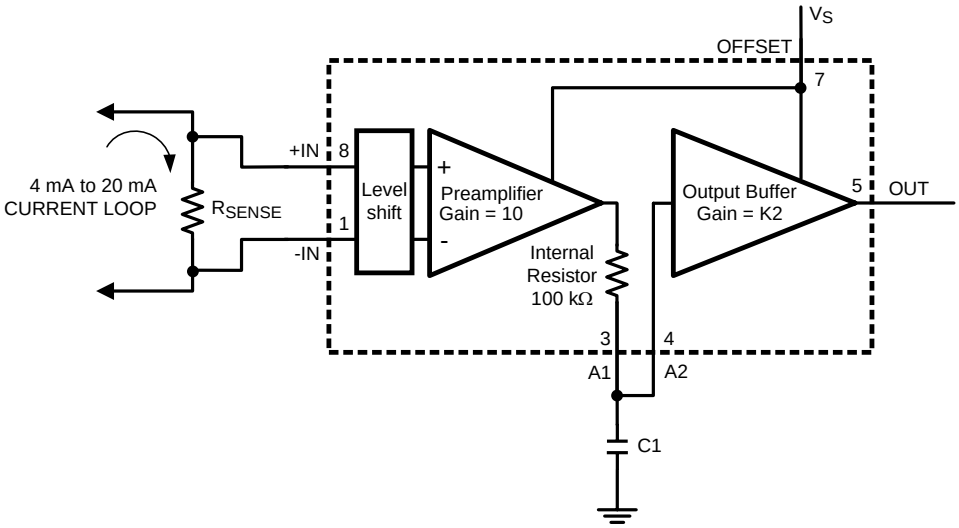
CURRENT LOOP RECEIVER APPLICATION

Many industrial applications use 4 to 20 mA transmitters to send a sensor's analog value to a central control room. The LMP8601/LMP8601Q can be used as a current loop receiver as shown in Figure 49.



K2 = 2

Figure 49. Current Loop Receiver Application

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F **Page**

- Added four typical curves 13

Changes from Revision D (March 2013) to Revision E **Page**

- Changed layout of National Data Sheet to TI format 23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8601MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01MA	Samples
LMP8601MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01MA	Samples
LMP8601QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01QMA	Samples
LMP8601QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01QMA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMP8601, LMP8601-Q1 :

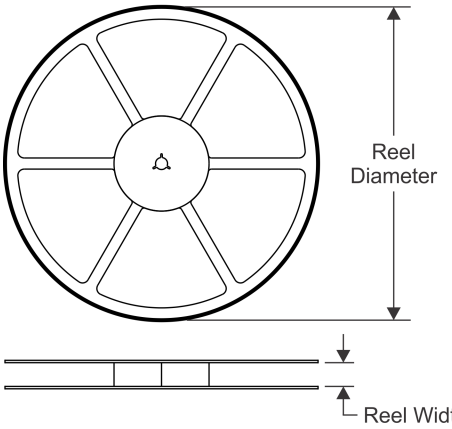
- Catalog: LMP8601
- Automotive: LMP8601-Q1

NOTE: Qualified Version Definitions:

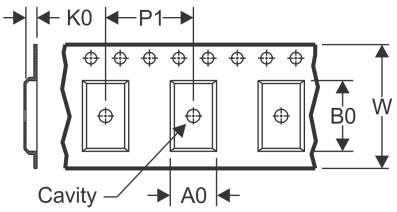
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

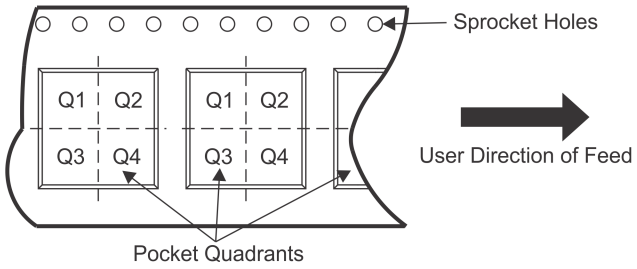


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

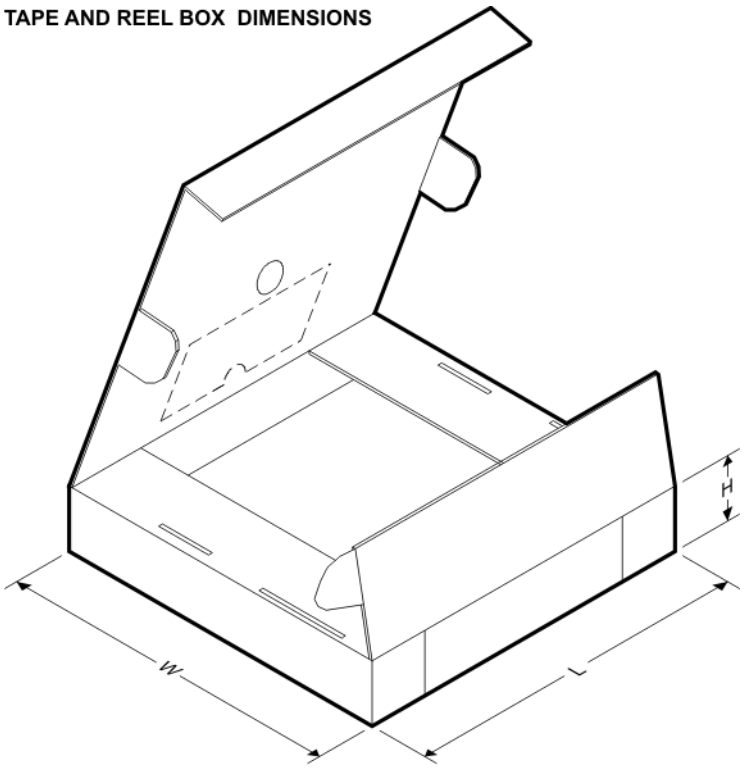
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8601MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8601QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

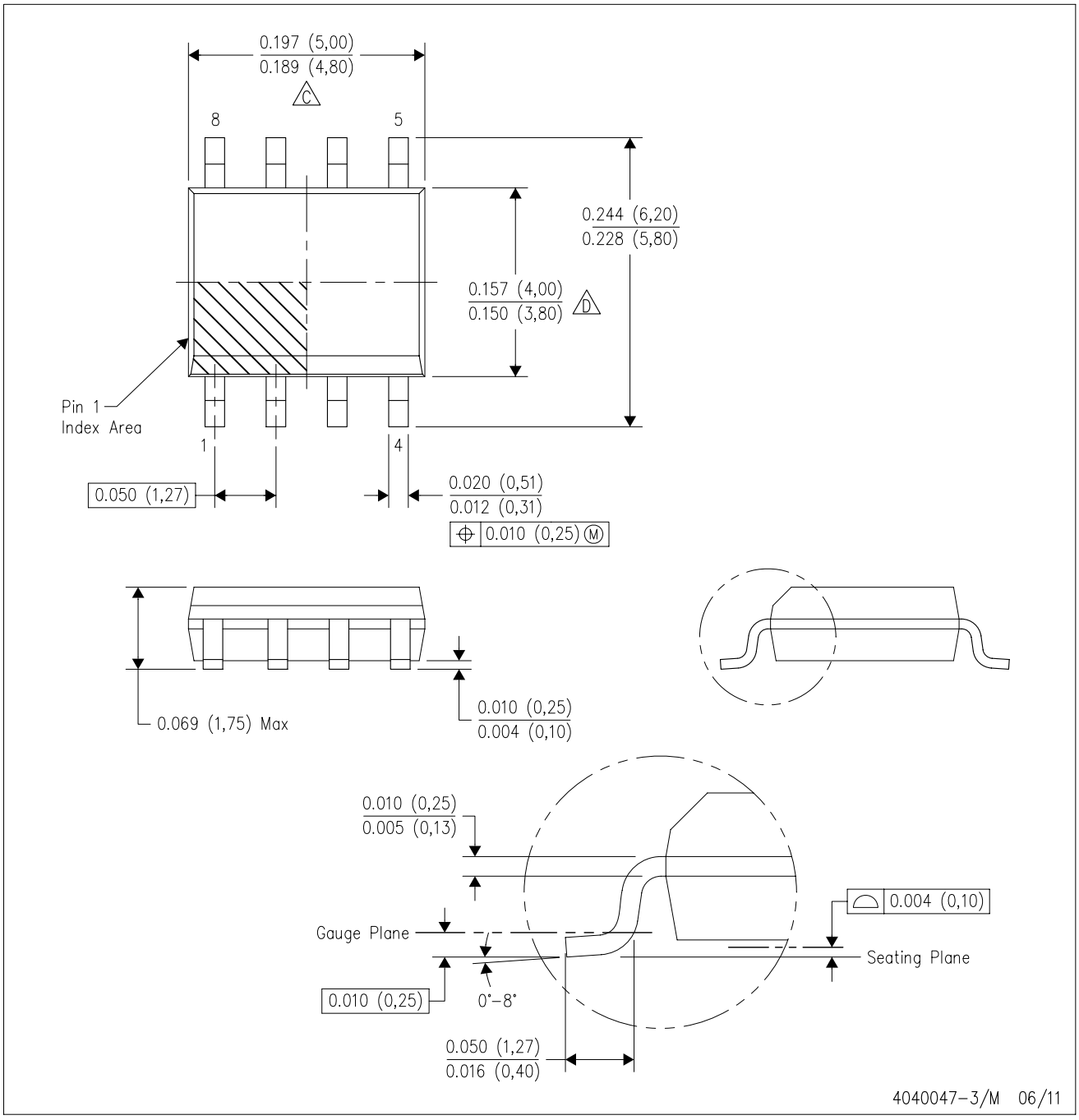
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8601MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8601QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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